What is claimed is:

1. A semiconductor device which is packaged at substantially identical outer dimensions to the outer dimensions of a first semiconductor chip, comprising:

first pads provided on a main surface of said first semiconductor chip;

a light-receiving element portion provided on said main surface of said first semiconductor chip such that a light-receiving surface thereof is exposed;

a light-transmitting portion provided so as to cover the light-receiving surface of said light-receiving element portion for transmitting incoming light to said light-receiving element portion;

a wiring layer which is electrically connected to said first pads and extends from said first pads over said main surface of said first semiconductor chip; and

external terminals which are provided in a position opposing said wiring layer and electrically connected to said first pads via said wiring layer.

2. A semiconductor device comprising:

a first semiconductor chip including a first main surface, a second main surface which opposes said first main surface and has a larger surface area than said first main surface, and side wall surfaces connecting said first main surface and second main surface;

first pads provided on the first main surface of said first semiconductor chip;

a light-receiving element portion provided on the first main surface of said first semiconductor chip such that a light-receiving surface thereof is exposed;

a light-transmitting portion provided so as to cover the light-receiving surface of said light-receiving element portion for transmitting incoming light to said light-receiving element portion;

a semiconductor chip carrying portion comprising a third main surface which includes a first region facing the second main surface of said first semiconductor chip and a second region which surrounds said first region, and a fourth main surface which opposes said third main surface;

a wiring layer which is electrically connected to said first pads and extends from said first pads, along said first main surface and said side wall surface, to said second region; and

external terminals which are provided over the second region and electrically connected to said first pads through said wiring layer.

3. A semiconductor device comprising:

a first semiconductor chip including a first main surface, a second main surface which opposes said first main surface and has a larger surface area than said first main surface, and side wall surfaces connecting said first main surface and second main surface;

first pads provided on the first main surface of said first semiconductor chip;

a light-receiving element portion provided on the first main surface of said first semiconductor chip such that a light-receiving surface thereof is exposed;

a light-transmitting portion provided so as to cover the light-receiving surface of said light-receiving element portion for transmitting incoming light to said light-receiving element portion;

a semiconductor chip carrying portion comprising a third main surface which includes a first region facing the second main surface of said first semiconductor chip and a second region which surrounds said first region, and a fourth main surface which opposes said third main surface;

a wiring layer which is electrically connected to said first pads and extends from said first pads, along said first main surface and said side wall surfaces, to said second region; and

external terminals provided over said fourth main surface side and electrically connected to said wiring layer via a conductive portion formed in a through hole which penetrates from the front to rear of said carrying portion.

4. The semiconductor device according to claim 3, wherein said light-transmitting portion is fixed in a position covering the light-receiving surface of said light-receiving element portion by a light-transmitting film serving as an adhesive layer, and

said light-transmitting film forms a sealing layer for burying and thereby sealing said first semiconductor chip.

5. The semiconductor device according to claim 3, wherein said light-transmitting portion is fixed in a position covering the light-receiving surface of said light-receiving element portion by a light-transmitting film serving as an adhesive layer which has a greater expansion coefficient than the expansion coefficient of said carrying portion,

a sealing layer for burying and thereby sealing said first semiconductor chip is provided on the lower side of said light-transmitting portion, and

said sealing layer on the upper side of said second region is formed by a sealing material having a smaller expansion coefficient than the expansion coefficient of said light-transmitting film.

6. The semiconductor device according to claim 3, wherein the surface area of a surface of said light-transmitting portion which opposes the light-receiving surface of said light-receiving element portion is formed to be greater than the surface area of the light-receiving surface of said light-receiving element portion, and

said light-transmitting portion comprises a convex portion and a concave portion provided on the periphery of said convex portion, said convex portion being disposed opposite said light-receiving surface and said concave portion being disposed opposite said wiring layer so as not to contact said wiring layer.

7. The semiconductor device according to claim 2, wherein said semiconductor chip carrying portion is set as a

second semiconductor chip, and this second semiconductor chip is electrically connected to said wiring layer.

8. The semiconductor device according to claim 3, wherein said semiconductor chip carrying portion is set as a second semiconductor chip, and this second semiconductor chip is electrically connected to said wiring layer.

9. A semiconductor device comprising:

a first semiconductor chip including a first main surface, a second main surface which opposes said first main surface and has a larger surface area than said first main surface, and a side wall surface for connecting said first main surface and said second main surface, the side wall surface having an inclined side wall surface formed by chamfering an edge portion between said side wall surface and said first main surface;

first pads provided on the first main surface of said first semiconductor chip;

a light-receiving element portion provided on the first main surface of said first semiconductor chip such that a light-receiving surface thereof is exposed;

a light-transmitting portion provided so as to cover the light-receiving surface of said light-receiving element portion for transmitting incoming light to said light-receiving element portion;

a frame-shape portion which comprises a third main surface and a fourth main surface opposing said third main surface, and which surrounds said first semiconductor chip such that at least a surface region of said inclined side wall surface

on said first main surface is exposed;

a wiring layer which is electrically connected to said first pads and extends from said first pads, along said first main surface and said inclined side wall surface, to said third main surface; and

external terminals provided over said third main surface and electrically connected to said first pads via said wiring layer.

10. The semiconductor device according to claim 1, further comprising:

post portions provided between said wiring layer and said external terminals; and

a sealing layer provided on said wiring layer and on the side surfaces of said post portions,

wherein an oxidation film is formed on the side surface of said post portions.

11. The semiconductor device according to claim 2, further comprising:

post portions provided between said wiring layer and said external terminals; and

a sealing layer provided on said wiring layer and on the side surfaces of said post portions,

wherein an oxidation film is formed on the side surface of said post portions.

12. The semiconductor device according to claim 9, further comprising:

post portions provided between said wiring layer and said

external terminals; and

a sealing layer provided on said wiring layer and on the side surfaces of said post portions,

wherein an oxidation film is formed on the side surface of said post portions.

13. The semiconductor device according to claim 2, wherein a part of said wiring layer positioned on a boundary between said first main surface and said side wall surfaces is formed to be wider than the remaining parts of said wiring layer.

14. The semiconductor device according to claim 3, wherein a part of said wiring layer positioned on a boundary between said first main surface and said side wall surfaces is formed to be wider than the remaining parts of said wiring layer.

15. The semiconductor device according to claim 9, wherein a part of said wiring layer positioned on a boundary between said first main surface and said side wall surface is formed to be wider than the remaining parts of said wiring layer.